Master of Technology in **VLSI Design**

Department of Electronics & Communication Engineering

Malaviya National Institute of Technology Jaipur

Subject Code	**Course Title**	**Credit Total (L T P)**
Semester 1 (Core Courses)		
ECT601	Digital CMOS ICs	3 (3-0-0)
ECT703	CAD Algorithms for Synthesis of VLSI Systems	3 (3-0-0)
ECT605	Digital System Design	3 (3-0-0)
ECT621	Semiconductor Devices	3 (3-0-0)
ECP611	System Design lab-1	3 (0-0-6)
ECT633	Analog IC Design	3 (3-0-0)
ECT990	Mathematical Methods & Techniques for ECE technologists-**I***	3 (3-0-0)
ECT992	Mathematical Methods & Techniques for ECE technologists-**II***	3 (3-0-0)
	Total Semester Credits	**21**
Semester 2 (2 + 5 electives)		
ECP612	System Design lab-2	3(0-0-6)
ECD656	Minor Project	4(0-0-8)
	(Elective Courses) #	
ECT614	VLSI Technology	3 (3-0-0)
ECT616	Computer Arithmetic & Micro-architecture Design	3 (3-0-0)
ECT618	Graph Algorithms & Combinatorial optimization	3 (3-0-0)
ECT622	System Level Design & Modeling	3 (3-0-0)
ECT624	VLSI Testing & Testability	3 (3-0-0)
ECT626	Formal Verification of Digital Hardware & Embedded Software	3 (3-0-0)
ECT628	Memory design & testing	3 (3-0-0)
ECT630	Advanced Computer Architecture	3 (3-0-0)
ECT632	Embedded SoC & Cyber Physical Systems	3 (3-0-0)
ECT634	Micro-& Nano- electro-mechanical Systems (MEMS & NEMS)	3 (3-0-0)
ECT638	Design of Asynchronous Sequential Circuits	3 (3-0-0)
ECT640	Electronic manufacturing Technology	3 (3-0-0)
ECT642	FPGAs Physical Design	3 (3-0-0)
ECT644	Mixed Signal IC Design	3 (3-0-0)

DPGC Convener Head, ECE SPGB Chairman

ECT648	Languages for Hardware Description, Scripting and Simulation	3 (3-0-0)
ECT649	Nanotechnology & Emerging Applications	3 (3-0-0)
ECT652	RF MEMS	3 (3-0-0)
ECT654	RF Integrated Circuits	3 (3-0-0)
ECT656	Adaptive Signal Processing	3 (3-0-0)
ECT657	VLSI signal processing architectures	3 (3-0-0)
ECT658	Current-Mode Analog Signal processing	3 (3-0-0)
Optional Electives (Over and Above)		
ECT643	Special modules in VLSI-I	1 (1-0-0)
ECT645	Special modules in VLSI-II	1 (1-0-0)
ECT646	Special modules in VLSI-III	1 (1-0-0)
ECT647	Special modules in VLSI-IV	1 (1-0-0)
	Total Semester Credits	**22**
Semester 3		
ECD659	Dissertation	16(0 0 32)
	Total Semester Credits	**16**
Semester 4		
ECD660	Dissertation	16(0 0 32)
	Total Semester Credits	**16**
	Total Credits of all semesters	**75**

#The students may opt for *any course from MTech (**ECE**) and selected courses form other MTech streams* in the Institute/department on recommendation of supervisor

*****Only one course out of ECT990 or ECT992 shall be opted by a student

DPGC Convener Head, ECE SPGB Chairman

Program: M. Tech. (VLSI Design)	**Department: Electronics & Communication Engineering**
Course Code: ECT601	**Course Name: Digital CMOS ICs**
Credit: 3	**L-T-P: 3-0-0**
Pre-requisite Course:	
Co-requisite Course:	

DPGC Convener Head, ECE SPGB Chairman

Syllabus:

Introduction to MOSFETs technology: Process flow and masking steps for MOS, Electrical behaviour of MOS transistors and CMOS fabrication technologies (well process, SOI and scaling), Latch up in CMOS technology. **[4h].**

CMOS Inverter: Design , analysis of NMOS inverter (resistive, enhancement and depletion load) , CMOS inverters; transfer characteristics, Noise margins, , rationing of transistor size, logic voltage levels, rise and fall of delays, Propagation Delay, Power Consumption. **[6h].**

Combinational Circuits: Design of basic gates in NMOS technology; CMOS logic design styles: static CMOS logic (NAND, NOR gates), complex gates, Pass Transistor logic, Transmission gate, Dynamic MOS design: pseudo NMOS logic, clocked CMOS (C2 MOS) logic, domino logic, NORA, Half and Full adder), Multiplexer, XOR, XNOR **[10h].**

Logical Effort: Logical Effort of Different Digital Circuit Design, Input capacitance, Logical and Electrical effort, parasitic delay, Single stage and Multistage with and without branch network. Design of minimum delay and optimization of best stages**.[5h]**

Layout and stick diagram: Layout Design Rules: Lambda and micron based design rules- stick diagram, Layer properties of various conducting layers in MOS and CMOS technology (diffusion, poly-silicon and metal), Layout design of different CMOS circuit, area estimation**.[5h]**

Sequential MOS Logic and Memory Design: Static latches; Flip flops & Registers, Dynamic Latches & Registers, CMOS Schmitt trigger, Monostable sequential Circuits, Astable Circuits. Memory Design: ROM & RAM cells **[10h].**

Project:

Introduction of open source tools: EDA. The class project is to design reasonably complex CMOS circuit. The project will be performed as a team of two or three students

References:

1. Sung-Mo Kang & Yusuf Leblebici, CMOS Digital Integrated Circuits Analysis and Design, Second Edition, McGraw-Hill, 1999.
2. Rabaey, Chandrakasan and Milokic. Digital system design- A design perspective. Pearson education, India.
3. Neil H.E.Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, A System Perspective, Pearson Education, India. 4. Ken Martin, Digital Integrated Circuits, Oxford Press.
4. CMOS Circuit Design, Layout and simulation: J. Baker, D.E. Boyce., IEEE press.

Course Outcomes:

At the end of the course the student will be able to:
CO1- Understand the advancement of CMOS devices and circuits (Cognitive- understanding)
CO2- Design CMOS circuits with specified noise margin and propagation delay. (Skills- Evaluate)
CO3- Implement efficient techniques at circuit level for improving power and speed of combinational and sequential circuits. (Skills- Analyze)
CO4- Design and optimization of layout for Digital ICs. (Skills-Creating)

Program: M. Tech. (VLSI Design)	**Department: Electronics & Communication Engineering**
Course Code: ECT703	**Course Name: CAD Algorithms for Synthesis of VLSI Systems**
Credit: 3	**L-T-P: 3-0-0**

DPGC Convener Head, ECE SPGB Chairman

Pre-requisite Course:

Co-requisite Course:

Syllabus:

Unit 1: **Introduction to CAD Algorithms**

Role of CAD in digital system design, levels of design, modeling & description and support of languages, RTL, gate and system level synthesis; Technological alternatives and technology mapping

Unit 2**: CAD Tools for synthesis**

CAD tools for synthesis, optimization, simulation and verification of design at various levels as well as for special realizations and structures such as microprogrammes, PLAs, gate arrays etc. Technology mapping for FPGAs. Low power issues in high level synthesis and logic synthesis.

Unit 3: **Architectural-Level Synthesis and Optimization**

Architectural Synthesis, Scheduling, Data path synthesis and control unit synthesis, scheduling algorithm, Resource Sharing and Binding

Unit 4: **Logic-Level Svnthesis and Optimization**

Two-Level Combinational Logic Optimization, Multiple-Level Combinational Logic Optimization, Sequential Logic Optimization

Unit 5: **CAD Algorithms for VLSI Physical Design**

Introduction to VLSI Physical Design flow. Circuit partitioning, placement and routing algorithms. Design Rule-verification, Circuit Compaction; Circuit Extraction and post layout simulation. FPGA design flow- partitioning, placement and routing algorithms. Deep sub-micron issues; interconnects modeling and synthesis

References:

1. G. D. Micheli. Synthesis and optimization of digital systems.
2. Dutt, N. D. and Gajski, D. D. High level synthesis, Kluwer, 2000.
3. T. H. Cormen, C. E. Leiserson and R. L. Rivest, “Introduction to Algorithms,” McGraw-Hill, 1990.
4. N. Deo, Graph Theory, PH India.
5. Sait, S. M. and Youssef, H. VLSI Physical design automation. IEEE press, 1995.
6. Sherwani, N. VLSI physical design automation. Kluwer, 1999.

Course Outcomes:

CO1: Is able to grasp various operations on graphs, clique, coloring, partitioning etc

& apply graph algorithms and its applications into Boolean function representation (Skills- Apply)

CO2: Is able to grasp graph models for architecture representation (Cognitive- understanding)

CO3: Is able to analyze & implement two level/Multilevel/ sequential logic synthesis algorithms

(approximate & exact algorithms) (skills- Analyze)

CO4: Is able to analyze & implement library binding algorithms- FSM equivalence & optimization (skills- Evaluate)

CO5: To able to grasp core concept of VLSI Physical Design algorithms. (Cognitive- Apply)

Program: M. Tech. (VLSI Design)	**Department: Electronics & Communication Engineering**
Course Code: ECT605	**Course Name: Digital System Design & FPGAs**
Credit: 3	**L-T-P: 3-0-0**

DPGC Convener Head, ECE SPGB Chairman

Pre-requisite Course:

Co-requisite Course:

Syllabus:

Sequential Logic Design- Introduction, Basic Bistable Memory Devices, additional bistable devices, reduced characteristics an excitation table for bistable devices.

Synchronous Sequential Logic Circuit Design- Introduction, Moore, Mealy and Mixed type Synchronous State Machines. Synchronous sequential design of Moore, Melay Machines,

Algorithmic State Machine- An Algorithm with inputs, digital solution, Implementation of traffic light controller, ASM charts, Design Procedure for ASMs.

Data path and Control design.

Introduction to VHDL/Verilog- Data types, Concurrent statements, sequential statements, behavioral modeling. Introduction to programmable logic devices- PALs, PLDs, CPLDs and FPGAs.

References:

1. Digital System Design, Ercegovac, Wiley.
2. Richard S. Sandige, *Modern Digital Design,* McGraw-Hill, 1990.
3. Zvi Kohavi, Switching and Finite Automata Theory, Tata McGraw-Hill.
4. Navabi. Analysis and modeling of digital systems. McGraw Hill, 1998.
5. Perry. Modeling with VHDL. McGraw Hill, 1994.
6. Navabi. Verilog Digital Design. McGraw Hill, 2007.
7. Fundamentals of Digital Logic with Verilog Design, Stephen Brown and Zvonko Vranesic, McGraw Hill, 2002.

Course Outcomes:

CO1: To be able to apply the basic design principles of sequential logic systems. (Cognitive- Applying)
CO2: To understand the design concepts of synchronous state machines in Moore and Mealy architectures. (Cognitive- understanding)
CO3: To analyze & design data path, control path design and various programmable devices (Skills- Create)
CO4: To be able to implement a digital system using HDLs (Skills- Evaluate)

Program: M. Tech. (VLSI Design)	**Department: Electronics & Communication Engineering**
Course Code: ECT621	**Course Name: Semiconductor Devices**
Credit: 3	**L-T-P: 3-0-0**
Pre-requisite Course:	

DPGC Convener Head, ECE SPGB Chairman

Co-requisite Course:

Syllabus:

Basic Semiconductor Physics : Crystal lattice, energy band model, density of states, distribution statics – Maxwell-Boltzmann and Fermi-Dirac, doping, carrier transport mechanisms, drift, diffusion, thermionic emission, and tunneling; excess carriers, carrier lifetime, recombination mechanisms – SHR, Auger.

p-n junction and metal-semiconductor junction: p-n junctions- fabrication, basic operation – forward and reverse bias, DC model, charge control model, I-V characteristics, steady-state and transient conditions, capacitance model, reverse-bias breakdown, SPICE model; metal-semiconductor junctions –fabrication, Schottky barriers, rectifying ad ohmic contacts, I-V characteristics.

MOS Capacitors and MOSFETs: The MOS capacitor – fabrication, surface charge, accumulation, depletion, inversion, threshold voltage, C-V characteristics – low and high frequency; MOSFET – fabrication, operation, gradual channel approximation, simple charge control model (SCCM), Pao-Sah and Schichman – Hodges models, I-V characteristics, second-order effects – Velocity saturation, short-channel effects, charge sharing model, hot-carrier effects, gate tunneling; subthreshold operation – drain induced barrier lowering (DIBL) effect, unified charge control model(UCCM), SPICE level 1, 2, and 3, and Berkeley short-channel model (BSIM).

MESFET and HEMTs: fabrication, basic operation, Shockley and velocity saturation models, I-V characteristics, high-frequency response, backgating effect, SPICE model; HEMTs – fabrication, modulation (delta) doping, analysis of III-V heterojunctions, charge control, I-V characteristics, SPICE model.

Advanced MOSFET technology: Partially and fully depleted SOI MOSFETs, high-k MOS devices, strained technology, metal gate electrode, FinFETs and Multi gate MOSFETs, enhanced quasi ballistic transport, Si Nanowire MOSFETs.

References:

1. Physics of Semiconductor Devices: *S. M. Sze, Wiley Eastern, (1981).*
2. Semiconductor physics and Devices, Donald Neamen, McGraw-Hill, 3rd edition.
3. Solid State Electronic Devices ,B.G.Streetman and S.Banerjee ,Prentice Hall India.
4. CMOS Circuit Design, Layout and simulation: *J. Baker, D.E. Boyce., IEEE press*.

Course Outcomes:

At the end of the course the student will be able to:
CO1- Understand the physical behavior of semiconductor devices. (Cognitive-Understanding)
CO2- Identify challenges of scaling in semiconductor devices. (Cognitive- Applying)
CO3- Compare performance metrics of semiconductor devices at different technology node. (Skills- Evaluate)
CO4- Design and Optimization of device for low power and high performance circuits. (Affective- Create)

Program: M. Tech. (VLSI Design)	**Department: Electronics & Communication Engineering**
Course Code: ECP611	**Course Name: System Design Lab - 1**
Credit: 3	**L-T-P: 0-0-6**
Pre-requisite Course:	

DPGC Convener Head, ECE SPGB Chairman

Co-requisite Course:

Syllabus:

Problem-set for algorithm implementation:

Boolean algebraic formulations

a. Covering algorithm- Brach & bound
b. ROBDD computation
c. Operation between ROBDDs: '+', '.'

Graph based optimization

a. Two consideration each
b. Two consideration each
c. Graph coloring
d. Clique partitioning
e. Edge covering
f. Vertex covering
g. Independent set finding

List scheduling

a. Latency constrained resource minimization
b. Resource constrained latency minimization
c. Path based scheduling
d. Pipelined data-path scheduling
e. Hu's multiprocessor scheduling

Allocation & binding

a. FU binding
    a. Coloring
    b. Clique finding
    c. Left edge based binding
b. Storage unit binding
    a. Coloring
    b. Clique finding
    c. Left edge based binding
c. Interconnect binding
    a. Coloring
    b. Clique finding
    c. edge based binding

Program: M. Tech. (VLSI Design)	**Department: Electronics & Communication Engineering**
Course Code: ECT633	**Course Name: Analog IC Design**
Credit: 3	**L-T-P: 3-0-0**
Pre-requisite Course:	

DPGC Convener Head, ECE SPGB Chairman

Co-requisite Course:

Syllabus:

Introduction to analog VLSI and analog design issues in CMOS technologies

Basic MOS Device Physics: Structure of MOSFET, Operation of MOSFET, MOS Device Models, **Active** resistors, current, voltage sources and sinks, Bandgap references.

Amplifiers: Common Source, Source follower, Common Gate and Cascode amplifiers, Biasing Techniques

Differential Amplifier-Basic differential Pair, common mode response, CMRR, Differential Pair with MOS load, Gilbert Cell.

Current Mirror- Basic Current Mirrors, Cascode Current mirror, Active Current mirror

Frequency Response of Amplifiers: Miller Effect, Association of Poles with nodes, Frequency Response of all single stage amplifiers, Cascode stage, Differential pair

Noise: Types of Noise, Noise in Single stage amplifiers, Current Mirrors, Differential pair

OPAMP Design: Single stage and Two Stage OPAMP, Stability and Frequency compensation

.

References:

1. Design of Analog CMOS Integrated Circuits: Behzad Razavi, McGraw Hill Education(India) Edition 2018
2. CMOS Circuit Design, Layout and simulation: *J. Baker, D.E. Boyce., IEEE press (2010).*
3. VLSI Design techniques for Analog and digital Circuits: *R.L. Geiger, P.E. Allen,* D. R. Holberg, OUP, (2/E) *McGraw Hill (2002)*
4. VLSI Design techniques for Analog and digital Circuits: Randel Geiger, P Allen, N Strader, Tata Mcgraw, Hill, (2/E) (2010)
5. Analysis And Design Of Analog ICs : Paul R. Gray, Paul J. Hurst Stephen H. Lewis, Robert G. Meyer, J, Willy and Sons, (4/E) (2001)

Course Outcomes:

At the end of the course the student will be able to:
CO1: Analyze and design amplifiers, current mirrors and differential amplifiers. (Skills- Analyze)
CO2: Understand the significance of different biasing techniques and apply them aptly to different circuits.(Cognitive- Understanding)
CO3: Comparatively evaluate the frequency response of single stage amplifiers, cascode amplifiers and differential amplifier circuits (Cognitive- Analyze)
CO4: Analyze and design two stage operational amplifier circuits (Skills- Create)
CO5: Understand basics of noise in different amplifier circuits (Cognitive- understand)
CO6: Analyze & design the compensation method of operational amplifiers for stability.(Skills- Evaluate)

Program: M. Tech. (VLSI Design)	**Department: Electronics & Communication Engineering**
Course Code: ECT990	**Course Name: Mathematical Methods and techniques for Electronics & Communication Technologists-I**
Credit: 3	**L-T-P: 3-0-0**

DPGC Convener Head, ECE SPGB Chairman

Pre-requisite Course:

Co-requisite Course:

Syllabus:

Advancements in Transforms: Discrete Fourier Transform, FFT, Short time Fourier Transform (STFT), Multi Resolution Analysis, Wavelet Transform, Continuous Wavelet Transform (CWT), Inverse CWT, Discrete Wavelet Transform, Sub-band coding and implementation of DWT, Applications (signal and image compression, de-noising, detection of discontinuous and breakdown points in signals), Discrete Cosine Transform, Stockwell-transform, Frequency selective filtering with wavelet and S-transform.

Modelling: Direct Modeling (identification), Inverse Modeling(Equalization), Classification and Clustering, Prediction/Forecasting, Auto regressive models (AR, MA, ARMA).

Optimization: Problem formulation, Linear Programming Problems, Solution by Graphical Methods, Symmetric Dual Problems, Slack and Surplus Variables, Simplex Method, Convex- Concave Problems.

Data Mining Techniques: Higher Order Statistics, Principal Component Analysis, Linear Discriminant Analysis, Independent Component Analysis

References:

1. Digital Signal Processing: Principles, Algorithms, and Applications 4 Edition, Author: John G. Proakis, Dimitris G Manolakis Publisher: Pearson.
2. Wavelets and Signal Processing, Author: Hans-Georg Stark, Publisher: Springer
3. The Wavelet Tutorial : The Engineer's Ultimate Guide to Wavelet Analysis, Author : Robi Polikar, University of Rowan : Online : http://users.rowan.edu/~polikar/WTtutorial.html
4. Stockwell, Robert Glenn, Lalu Mansinha, and R. P. Lowe. "Localization of the complex spectrum: the S transform." IEEE Transactions on Signal Processing 44.4 (1996): 998-1001.
5. Engineering Optimization: Theory and Practice, Third Edition SINGIRESU S. RAO, New Age Publishers
6. Data Mining - Concepts and Techniques, Authors : Jain Pei, Jiawei Han, Micheline Kamber, Publisher : Elsevier

Course Outcomes:

CO1. To learn the advancement in transforms
CO2. To understand the mathematical modeling and optimization techniques.
CO3. To learn the data mining techniques
CO4. To explore the engineering applications of the mathematical techniques.
CO5. To develop MATLAB and other programming skills for the mathematical techniques realization.

Program: M. Tech. (VLSI Design)	**Department: Electronics & Communication Engineering**
Course Code: ECT992	**Course Name: Mathematical Methods and techniques for Electronics & Communication Technologists-II**
Credit: 3	**L-T-P: 3-0-0**

DPGC Convener Head, ECE SPGB Chairman

Pre-requisite Course:

Co-requisite Course:

Syllabus:

[The following contents intend to cover implicit application to and exemplification through ECE problems in Electronic systems/Cognitive-systems domain such as reduced order polynomials, order reduction of a transfer function, sparse matrix based solution of large systems, discrete structures, implementation of search algorithms for design space exploration, and computer arithmetic implementation along with probabilistic reasoning for AI]

A. (i) (a) Large Matrix analysis and large Eigen value problem– Groups, fields and rings; vector spaces; basis & dimensions; canonical forms; inner product spaces- orthogonalization, Gram-Schmidt orthogonalization, unitary operators, change of orthonormal basis, diagonalization; (b) Eigenvalues & eigen vectors- Gerschghorin theorem, iterative method, Sturm sequence, QR method, introduction to large Eigen value problems. 08 Hrs.

(ii) Reduced order modelling of systems- Taylor's polynomial, least square approximation, Chebyshev series/polynomial, splines, Pade & rational approximation 04 Hrs.

B. Discrete Structures, graphs, algorithms & Combinatorial optimization- counting methods, algorithm analysis, graph algorithms, dynamic algorithms, randomized algorithms, probabilistic algorithms, combinatorial optimization16 Hrs.

C. (i) Number theory & computer arithmetic- unconventional number systems, residue number system, logarithmic number system, Chinese remainder theorem; fast evaluation of elementary & transcendental arithmetic functions. 06 Hrs.

(ii) Preface to AI- first order logic & inferencing, uncertainty, probabilistic reasoning systems, making decisions under uncertainty; ***08 Hrs.***

References:

1. Schaum's outline on Linear Algebra, McGraw Hill
2. Topics in Algebra, I. N. Herstein, Wiley.
3. Gerald, C F; Wheatley P O; Applied Numerical Analysis, Pearson, 2017
4. Theory and Applications of Numerical Analysis, G. M. Phillips, Peter J. Taylor, Academic press
5. Advanced Model Order Reduction Techniques in VLSI Design, Sheldon Tan, Lei He, Cambridge Univ. Press, 2007.
6. Cormen, Rivest, Leiserson, Introduction to Algorithms, PHI
7. Combinatorial optimization, Papadimitriou and Steiglitz, PHI (I)
8. Russel and Norvig- Artificial Intelligence: A Modern Approach, Pearson, 3rd Ed. 2017
9. Israel Koren, Computer Arithmetic- Academic Press
10. Model Order Reduction: Theory, Research Aspects and Applications edited by W. H. A. Schilders, Henk A. Van Der Vorst, Joost Rommes, Springer.
11. Discrete Structures, Schaum outline

Further references

1. MODEL ORDER REDUCTION TECHNIQUES WITH APPLICATIONS IN ELECTRICAL ENGINEERING**,** Luigi FORTUNA, Guiseppe NUNNARI, Antonio GALLO, Springer, 1992.
2. Y. Saad, Numerical methods for large Eigenvalue problems, www.umn.edu
3. Matrix Analysis & linear algebra, Meyer, SIAM
4. H. A. van der Vorst, Iterative methods for large linear systems, citeseerx.ist.psu.edu

Course Outcomes:

CO1. Is able to grasp core concepts, basic tenets of linear algebraic structures- groups, fields and rings;vector spaces (knowledge)

CO2. Is able to grasp features, properties and operations on vector spaces- orthogonalization, change of basis, diagonalization (knowledge)

CO3. Is able to learn & apply problem solving for computing eigen values and eigen vectoraetc. (Thinking, skills)

CO4. Is able to demonstrate application of algorithms (Gerschgorin, Sturm sequence method, QR method) for eigen value computation/estimation and MATLAB validation(skills)

CO5. Is able to describe algorithms for function approximation (rational, Chebychev, Pade etc.) using

MATLAB (skills)

CO6. Develops appreciation for combinatorial optimization algorithms, AI probabilistic approaches & implements through MATLAB/C++ (skills)

DPGC Convener Head, ECE SPGB Chairman

Program: M. Tech. (VLSI Design)	Department: Electronics & Communication Engineering
Course Code: ECP612	**Course Name: System Design Lab - 2**
Credit: 3	**L-T-P: 0-0-6**
Pre-requisite Course:	
Co-requisite Course:	

Syllabus:

S. No	*Objective Of Experiment*
A-1	Layout Design- (i) Full adder, D-FF ; & (ii) synthesis of combinational & Sequential Components- 4-bit adder, 4-bit shift register, sequence detector ("1010")
A-2	Layout synthesis of already designed (1^{st} Odd Semester) Data Path & Control for an arithmetic/logic application. Synthesis Using SYNOPSYS/CADENCE tool

Individual Application/Problems:

1. GCD-computer (4-bit)
2. Booth multiplier (4-bit)
3. 4-pt FFT
4. 4-pt IFFT
5. CORDIC for SinΘ/CosΘ
6. CORDIC for $Sin^{-1}Θ/Cos^{-1}Θ$
7. Non-Linear function exp(-2.5)/Sin 1.45/ Cos3.1/Sinh2.5/ Cosh3.2/log-natural
8. Find Average of Floating Point Numbers in Array of Size 16/32/64/128

1. For pseudo exhaustive TPG set T for BIST, follow the theorem concerning logical segmentation, which relates n (inputs), k (subspaces of size k among n), w (weight of n-tuple). Indicate w as well as $|T_c|$ for different c; and n=20, k=3. Take example circuits/sub-systems for implementing the scheme & generating/applying random test patterns.
2. A circuit implementing f=xy+yz is to be tested using the syndrome-test method. Show that the faults z s-a-0 and z s- a-1 are not detected, while all other single stuck-at faults are detected. Arrange for experimental setup for all such testable as well as non-testable faults.
3. In a shift register polynomial division method of compression, a type 2 LFSR with $P^*(x)=1+x^2+x^4+x^5$ is to be used for input sequence 1 1 1 1 0 1 0 1 (8 bits). Compute signature for the input sequence. Indicate at least one more input sequence, which would alias the given sequence. Arrange for experimental setup for verifying your design.

DPGC Convener Head, ECE SPGB Chairman